



## P61089Q



硬件可编程过电压保护集成电路

版本号  
201603-A

### 产品概述

P61089Q 主要用于保护 SLIC 免遭瞬态过电压冲击。正向过载由两个二极管来控制，负向浪涌由两个晶闸管抑制，晶闸管的动作电压与门极电压 $-V_{BAT}$ 有关。该器件有非常低的门极触发电流 ( $I_{GT}$ ) 以减少电路工作时的损耗。器件结构如图 1 所示。“四点”结构保证了高可靠的保护，特别是针对非常快速的瞬间线感应过压 ( $L \cdot di/dt$ ) 图 1 和图 2 分别为器件的等效结构图和外型图。

### 产品特点

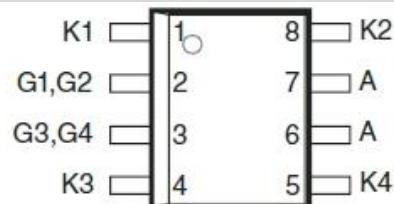
- 双编程瞬态抑制；
- 负压范围宽： $V_{MGL}=-170V_{MAX}$
- 动态开关电压低： $V_{FP}$  和  $V_{DGL}$
- 门极触发电流低： $I_{GT}=5mA_{Max}$
- 峰值脉冲电流： $I_{PP}=40A$  (10/700μs)
- 维持电流： $I_H \geq 150mA$

### 应用领域

P61089Q 主要应用于程控交换机等通讯设备的二级过电压防护。

### 特征参数

符号	额定值	单位
$V_{MGL}$	-170	V
$I_{PP}(10/700)$	40	A
$I_H$	150	mA



### 封装：SOP-8

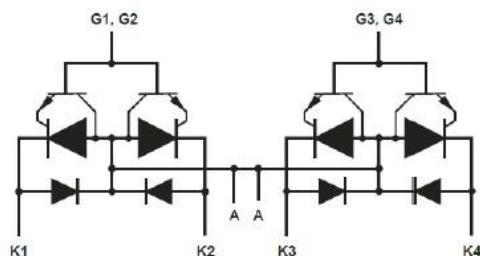


图1、器件等效结构图

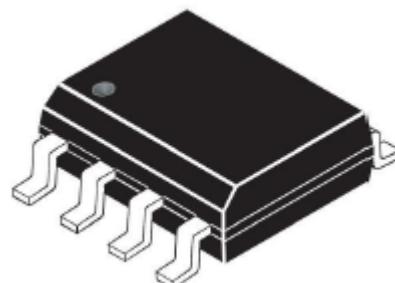


图2、器件外型图 SOP-8



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## ■ 满足标准

标准类型	波形		ITSP
ITU-T K.20/21 和 K.45	电压	10/700μs	40A
	电流	5/310μs	

## ■ 电特性

● 极限值 除非另有规定  $T_a = 25^\circ\text{C}$

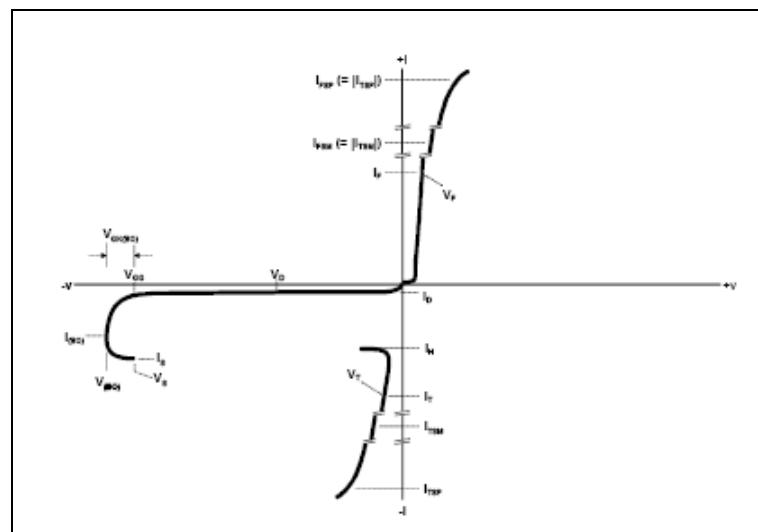
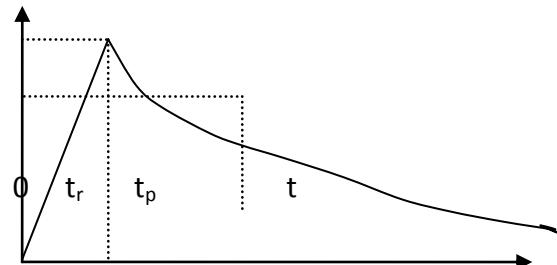
符号	参数	数值	单位
$V_{PP}/I_{PP}$	峰值脉冲电压/电流 (注1)	10/700μs	V
		5/310μs	A
$I_{TSM}$	非重复性浪涌峰值电流 ( $f=50\text{Hz}$ )	$t_p=10\text{ms}$	A
		$t=1\text{s}$	
$I_{GSM}$	最大门极电流 (半正弦波 $t_p=10\text{ms}$ )	2	A
$V_{MLG}$	线—地间最大电压	-170	V
$V_{MGL}$	门极—线间最大电压	-170	V
$T_{stg}$	存储温度范围	-55~150	°C
$T_j$	最高温度	150	°C
$T_L$	10 秒内可承受的最高焊锡温度	260	°C

注 1: 脉冲波形:

5/310μs  $t_r=5\mu\text{s}$   $t_p=310\mu\text{s}$  100% $I_{PP}$

● 伏安特性曲线 ( $T_a = 25^\circ\text{C}$ )

符号	参数
$I_{GT}$	门极触发电流
$I_H$	维持电流
$I_{RM}$	线—地间反向漏电流
$I_{RG}$	门极—线间反向漏电流
$V_{RM}$	线—地间反向电压
$V_F$	线—地间正向电压
$V_{GT}$	门极触发电压
$V_{FP}$	线—地间正向峰值电压
$V_{DGL}$	门极—线间动态开关电压
$V_{GATE}$	门极—地间电压
$V_{LG}$	线—地间电压
C	线—地间断态电容





I <sub>H</sub>	维持电流	
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■ 电参数 除非另有规定, T<sub>a</sub>=25°C

● 线地间二极管相关参数

符 号	测 试 条 件	最 大 值	单 位
V <sub>F</sub>	I <sub>F</sub> =5A, t <sub>p</sub> =500μs	3	V
V <sub>FP</sub>	10/700μs 1.5kV R <sub>P</sub> =10Ω (见注释 1)	5	V

注释 1: V<sub>FP</sub> 见测试电路 2, R<sub>P</sub> 是装在线卡上的保护电阻

● 保护晶闸管相关参数 (T<sub>a</sub>=25°C)

符 号	测 试 条 件	最 小 值	最 大 值	单 位
I <sub>GT</sub>	V <sub>GND/LINE</sub> =-100V	0. 1	5	mA
I <sub>H</sub>	V <sub>GATE</sub> =-100V	150		mA
V <sub>GT</sub>	同 I <sub>GT</sub>		2. 5	V
I <sub>RG</sub>	T <sub>C</sub> =25°C V <sub>RG</sub> =-75V		5	μA
	T <sub>C</sub> =70°C V <sub>RG</sub> =-75V		50	
V <sub>DGL</sub>	V <sub>GATE</sub> =-100V (见注释 3) 10/700μs 1.5kV R <sub>P</sub> =10Ω		10	V

注释 2: 见测试电路 2 功能维持电流 (I<sub>H</sub>);

注释 3: 见测试电路 1 关于 V<sub>DGL</sub>, 波动时间小于 50ns 不作记录。

● 保护晶闸管和二极管相关参数

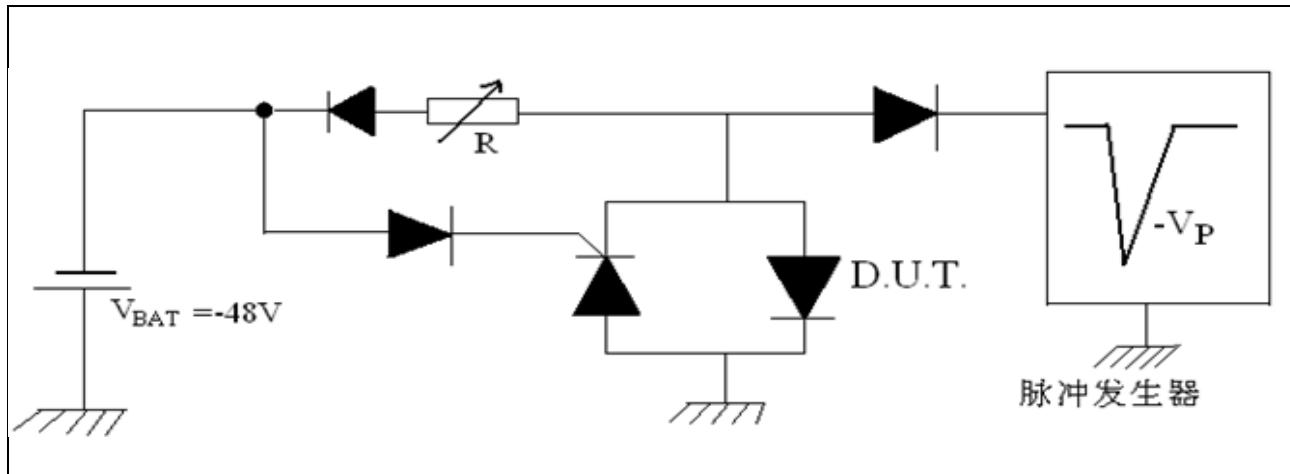
符 号	测 试 条 件	最 大 值	单 位
I <sub>RM</sub>	T <sub>C</sub> =25°C V <sub>GATE/LINE</sub> =-1V V <sub>RM</sub> =-75	5	μA
	T <sub>C</sub> =70°C V <sub>GATE/LINE</sub> =-1V V <sub>RM</sub> = -75	50	μA
C	V <sub>R</sub> =-3V F=150KHz	100	P <sup>F</sup>
	V <sub>R</sub> =-48V F=150KHz	50	P <sup>F</sup>





## ■ 测试方法及电路

### ● 维持电流测试电路（测试电路 1）

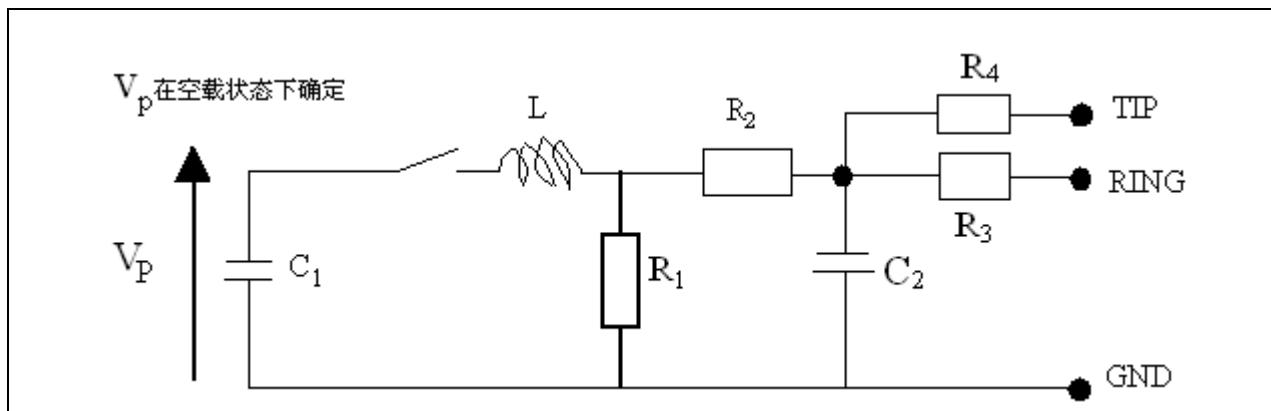


这是一个“导通-截止”测试，该测试电路可以确定维持电流的大小。

测试方法：

- ① 短路 DUT，调节电流在  $I_h$  值范围；
- ② 用  $I_{PP}=10A, 10/1000\mu s$  的浪涌电流触发 DUT；
- ③ DUT 最多在 50ms 内必须返回到断态。

### ● $V_{FP}$ 和 $V_{DGL}$ 参数测试电路 2





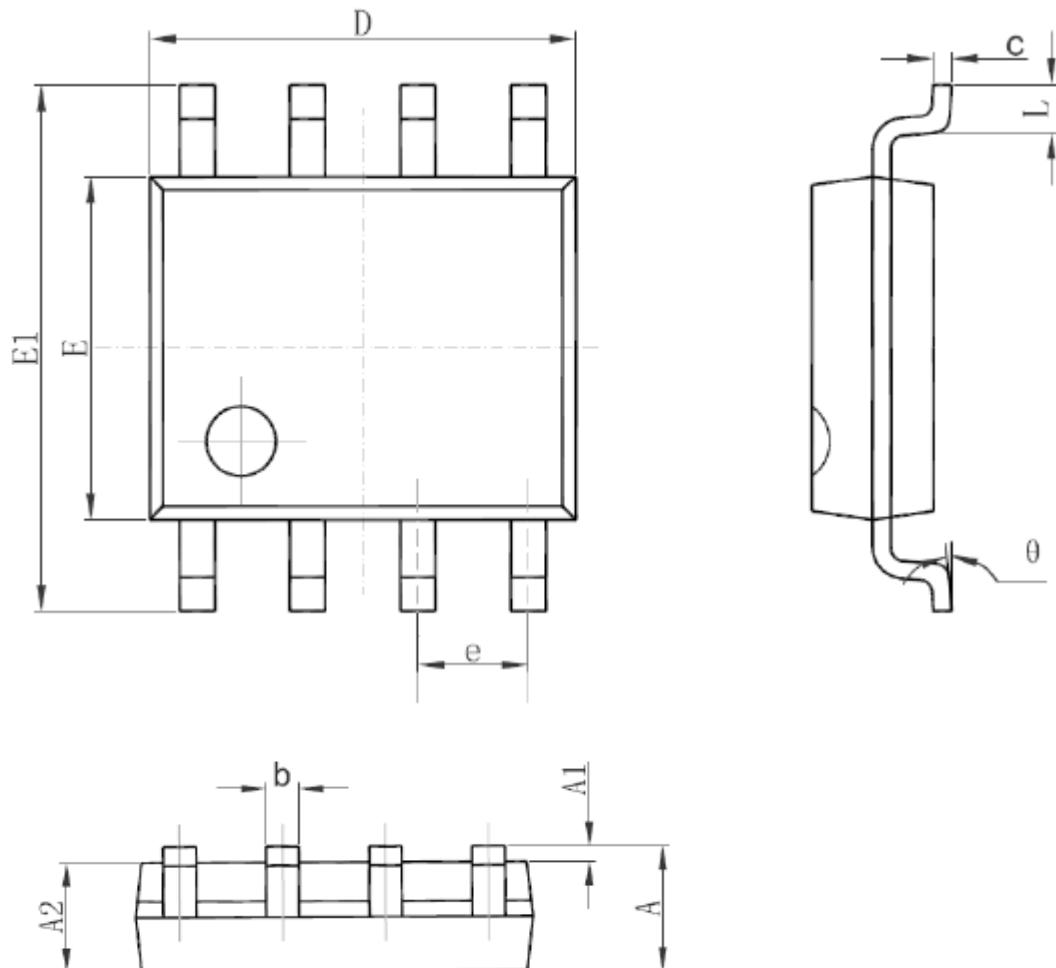
Pluse(μs)		V <sub>P</sub> (V)	C <sub>1</sub> (μF)	C <sub>2</sub> (nF)	L (μH)	R <sub>1</sub> (Ω)	R <sub>2</sub> (Ω)	R <sub>3</sub> (Ω)	R <sub>4</sub> (Ω)	I <sub>PP</sub> (A)	R <sub>P</sub> (Ω)
t <sub>r</sub>	t <sub>p</sub>										
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62





## 封装尺寸

### ■ 外观尺寸图 SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



## ■ 打印标示

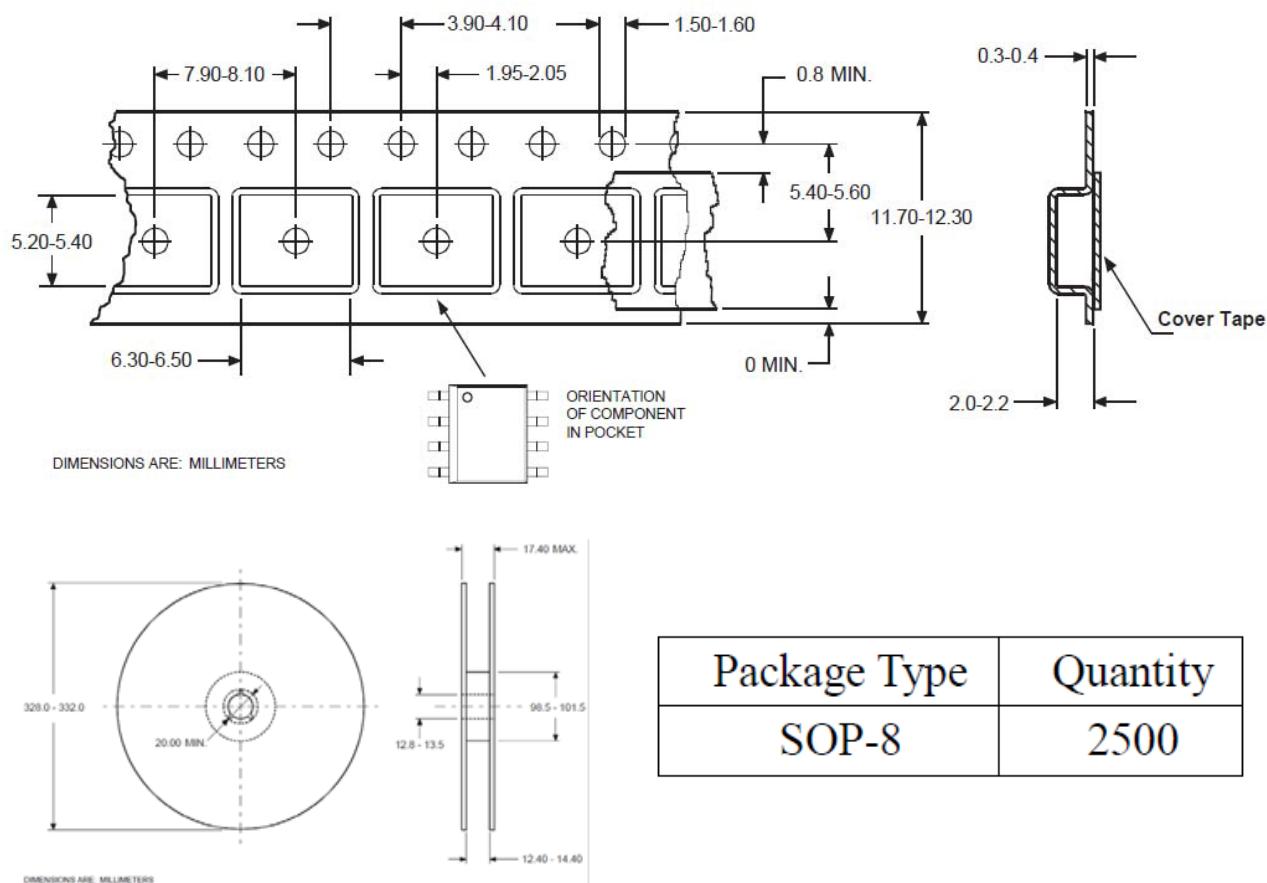


## ■ 命名规则



XXYY:XX表示年份， YY表示星期。

## ■ 编带规范



	<b>P61089Q</b>	版本号 201603-A
	<b>Dual Programmable Thyristor Transient Voltage Suppressor</b>	

## Description

This device has been especially designed to protect 2 new high voltage, as well as classical SLICs, against transient overvoltages. Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to  $-V_{BAT}$  through the gate. This component presents a very low gate triggering current in order to reduce the current consumption on printed circuit board the firing phase. This devices are not subject to aging and provide a fail safe mode in short circuit for a better protection. Pic 1 and pic 2 are the device symbol and the package.

## Features and Benefits

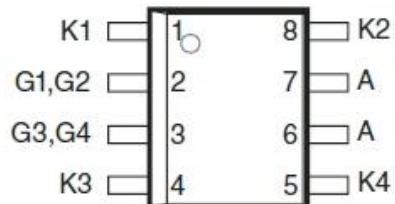
- Dual Voltage-Tracking Protectors ;
- wide negative pressure range:  $V_{MGL} = -170V_{MAX}$
- low dynamic switching voltage:  $V_{FP}$  and  $V_{DGL}$
- low gate triggering current :  $I_{GT} = 5mA_{Max}$
- Peak Pulse Current:  $I_{PP} = 40A$  ( $10/700\mu s$ )
- high Holding current :  $I_H \geq 150mA$

## Application field

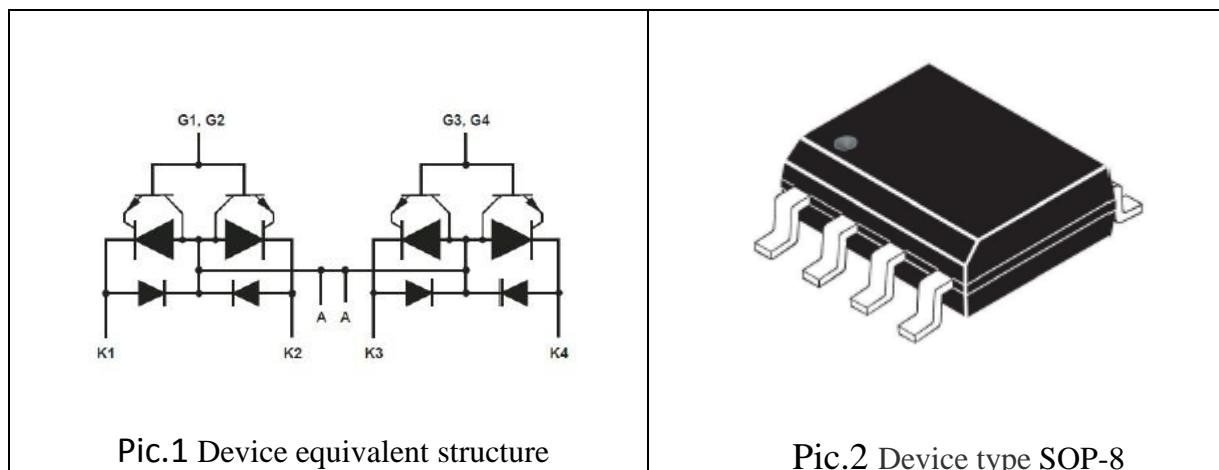
P61089Q are designed to protect communication equipment such as SPC exchanger from damaging overvoltage transients in the second level.

## Characteristic parameters

symbol	Rated value	unit
V <sub>MGL</sub>	-170	V
I <sub>PP</sub> (10/700μs)	40	A
I <sub>H</sub>	150	mA



Package : SOP-8



Pic.1 Device equivalent structure

Pic.2 Device type SOP-8

## Electrical Parameters

### ■ Standard

type	Wave shape		ITSP
ITU-T K.20/21and K.45	voltage	10/700μs	40A
	current	5/310μs	

### ■ Electrical characteristics

- Absolute maximum ratings T<sub>a</sub> = 25°C unless otherwise noted

symbol	parameters	value	unit
V <sub>PP</sub> /I <sub>PP</sub>	Peak pulse voltage /current (tip.1)	10/700μs	V
		5/310μs	A
I <sub>TSM</sub>	Non repetitive peak pulse current (F=50Hz)	t <sub>p</sub> =10ms	A
		t=1s	
I <sub>GSM</sub>	Maximum gate current (half sinusoidtp=10ms)	2	A
V <sub>MLG</sub>	Line-ground maximum voltage	-170	V
V <sub>MGL</sub>	Gate-line maximum voltage	-170	V
T <sub>stg</sub>	Storage Temperature Range	-55~150	°C
T <sub>j</sub>	maximum temperature	150	°C
T <sub>L</sub>	maximum sustainable temperature of solder in 10 seconds	260	°C

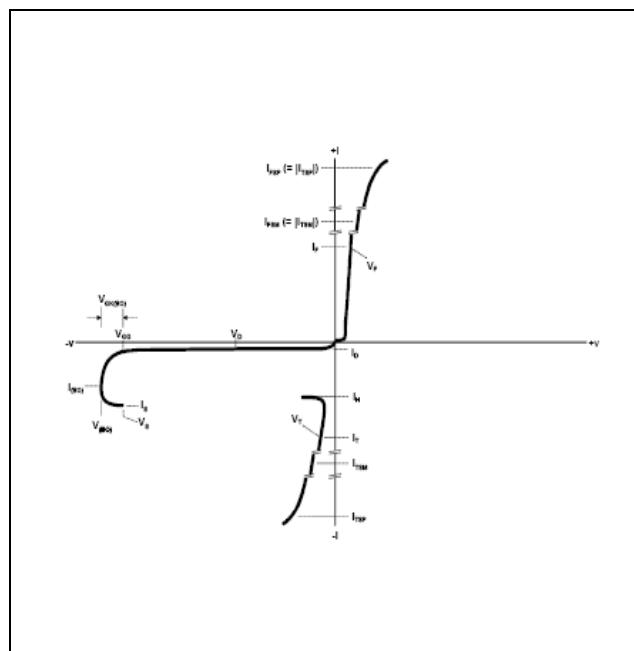
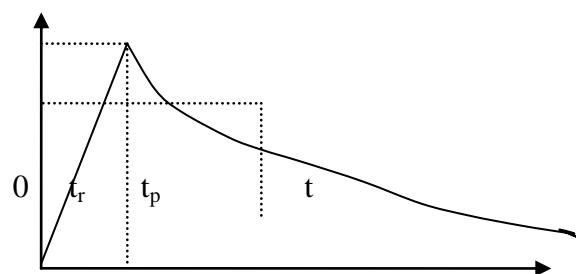


tip.1: pulse form:

$5/310\mu s$   $t_r=5\mu s$   $t_p=310\mu s$   $100\% I_{PP}$

● V-I characteristic curve ( $T_a = 25^\circ C$ )

symbol	parameters
$I_{GT}$	Gate trigger current
$I_H$	Holding current
$I_{RM}$	Line-ground reverse leakage current
$I_{RG}$	Gate-line reverse leakage current
$V_{RM}$	Line-ground reverse voltage
$V_F$	Line-ground voltage
$V_{GT}$	gate trigger voltage
$V_{FP}$	Line-ground peak voltage
$V_{DGL}$	Gate-line dynamic switching voltage
$V_{GATE}$	Gate-ground voltage
$V_{LG}$	Line-ground voltage
C	Line-ground off state capacitance



### Electrical Parameters

Absolute maximum ratings  $T_a = 25^\circ C$  unless otherwise noted

● Line-ground diode parameters

symbol	Test conditions	Max.	unit
$V_F$	$I_F=5A, t_p=500\mu s$	3	V
$V_{FP}$	$10/700\mu s \ 1.5kV \ R_P=10\Omega$ (tip. 1)	5	V

tip.1:  $V_{FP}$  refers to test circuit 2,  $R_P$  is the protective resistance mounted on the card

● thyristor parameters ( $T_a=25^\circ C$ )



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symbol	Test conditions	Min.	Max.	unit
I <sub>GT</sub>	V <sub>GND</sub> /L <sub>INE</sub> =-100V	0.1	5	mA
I <sub>H</sub>	V <sub>GATE</sub> =-100V	150		mA
V <sub>GT</sub>	Same to I <sub>GT</sub>		2.5	V
I <sub>RG</sub>	T <sub>C</sub> =25°C V <sub>RG</sub> =-75V		5	μA
	T <sub>C</sub> =70°C V <sub>RG</sub> =-75V		50	
V <sub>DGL</sub>	V <sub>GATE</sub> =-100V (TIP.3) 10/700 μs 1.5kV R <sub>P</sub> =10Ω		10	V

Tip.2: see holding current (I<sub>H</sub>) at test circuit 2;

Tip.3: see V<sub>DGL</sub> at test circuit 1, Don't make records if fluctuation time is less than 50ns.

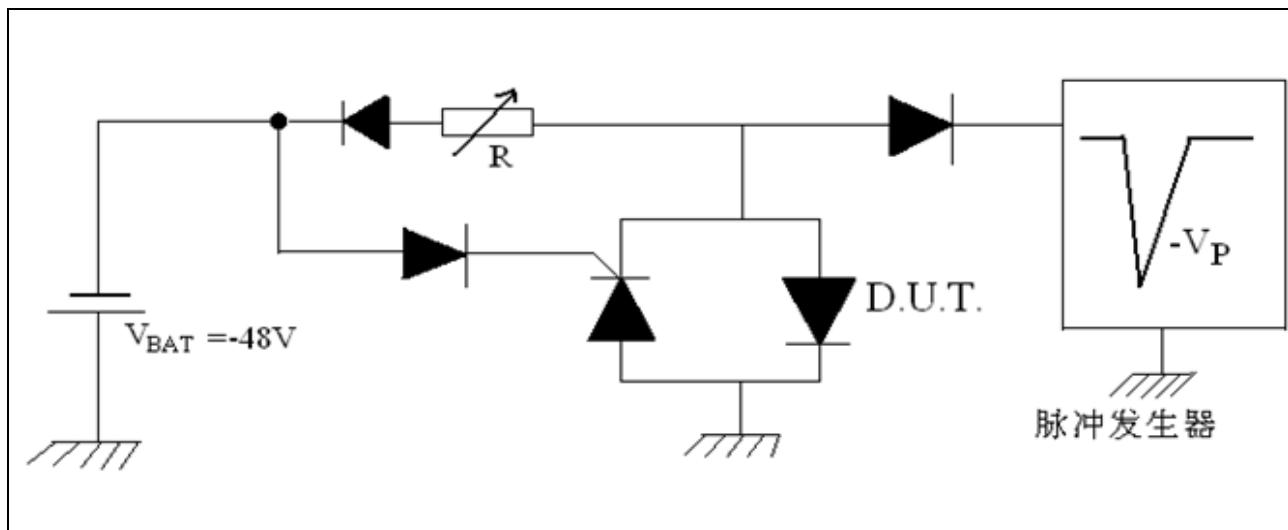
- thyristor and diode parameters

Symbol	Test conditions	Max.	unit
I <sub>RM</sub>	T <sub>C</sub> =25°C VGATE/LINE=-1V V <sub>RM</sub> =-75	5	μA
	T <sub>C</sub> =70°C VGATE/LINE=-1V V <sub>RM</sub> = -75	50	μA
C	V <sub>R</sub> =-3V F=150KHz	100	P <sup>F</sup>
	V <sub>R</sub> =-48V F=150KHz	50	P <sup>F</sup>



## ■Test method and circuit

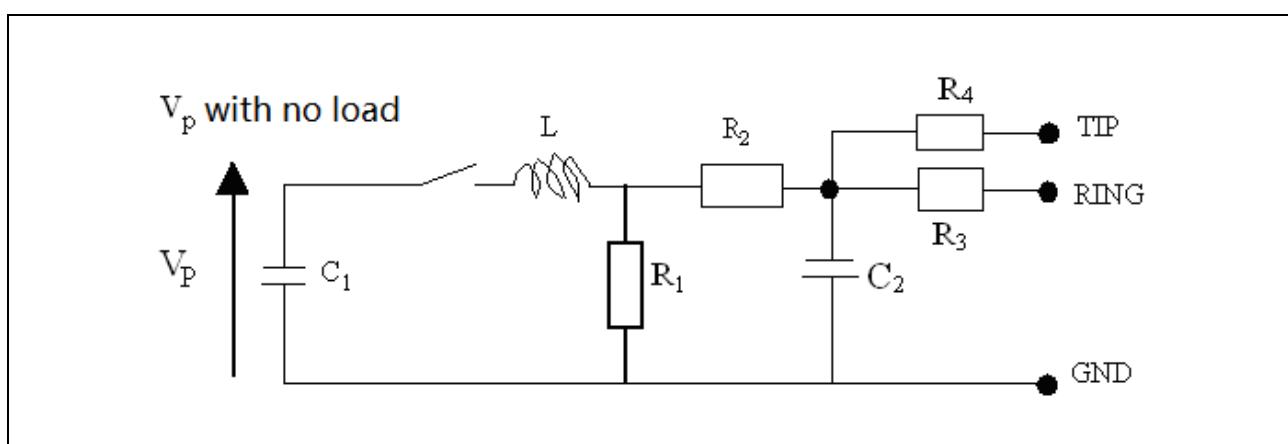
- Holding current test circuit (test circuit1)



This is a “Conducting-cutoff” test. The test circuit can ascertain the size of holding current.

### Test method :

- ① short out DUT, regulating current in  $I_H$  range;
  - ② let  $I_{PP}=10A$ ,  $10/1000\mu s$  surge current triggers DUT;
  - ③ DUT must return to the off-state in  $50ms$ .and
- $V_{FP}$  and  $V_{DGL}$  test circuit2

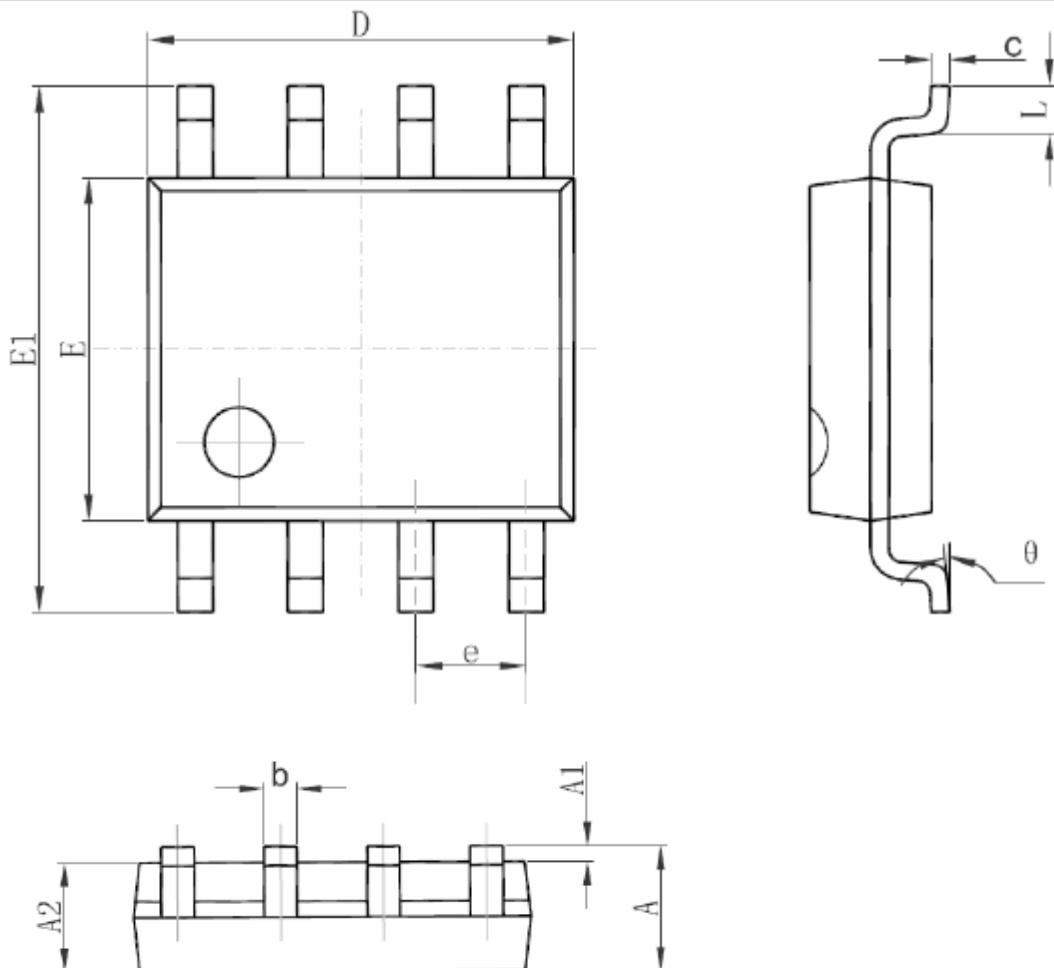


Pluse(μs)		$V_p$ (V)	$C_1$ (μF)	$C_2$ (nF)	$L$ (μH)	$R_1$ (Ω)	$R_2$ (Ω)	$R_3$ (Ω)	$R_4$ (Ω)	$I_{PP}$ (A)	$R_p$ (Ω)
$t_r$	$t_p$										
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62



## Package size

### ■ Appearance size SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



## Marking

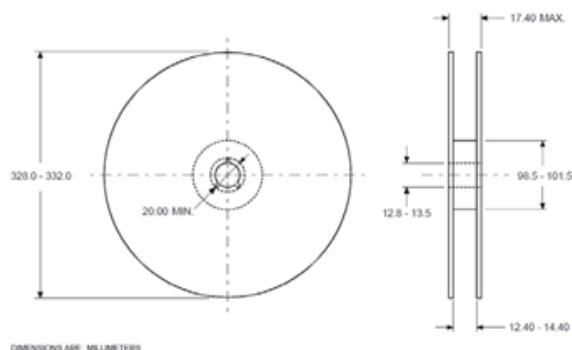
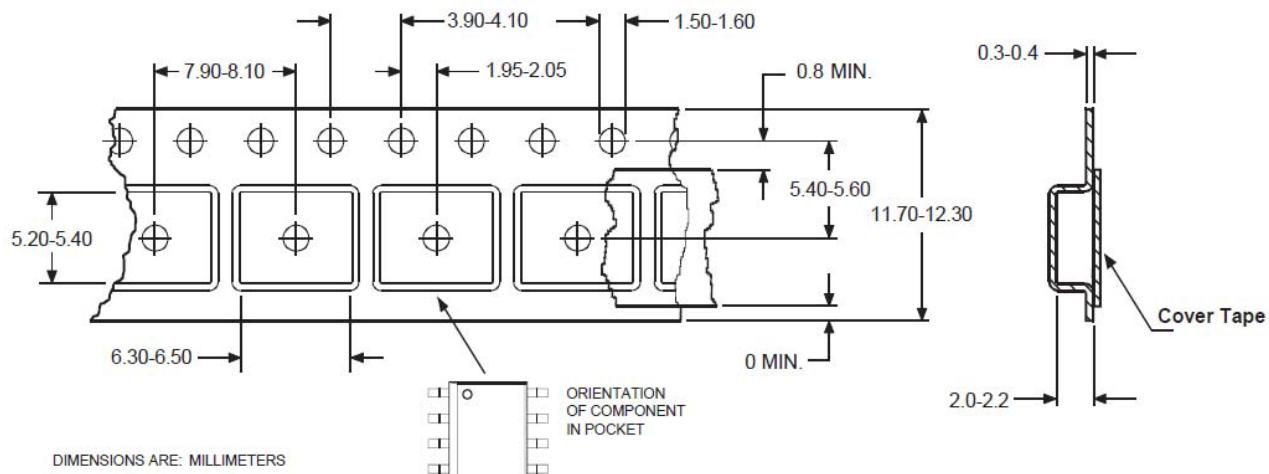


## Naming Rule



XXYY:XX means year, YY means week.

### ■ Package Information



Package Type	Quantity
SOP-8	2500

